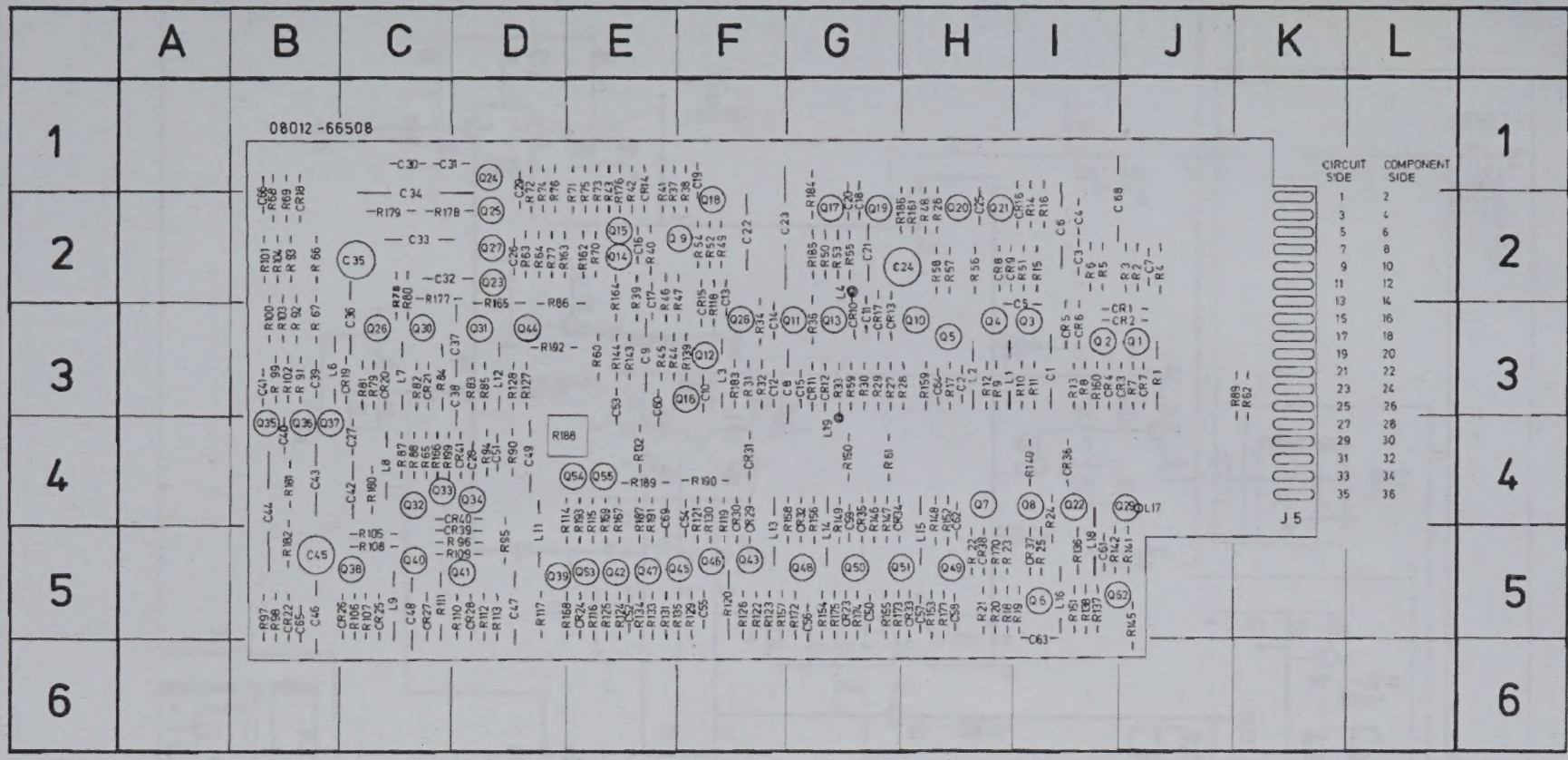
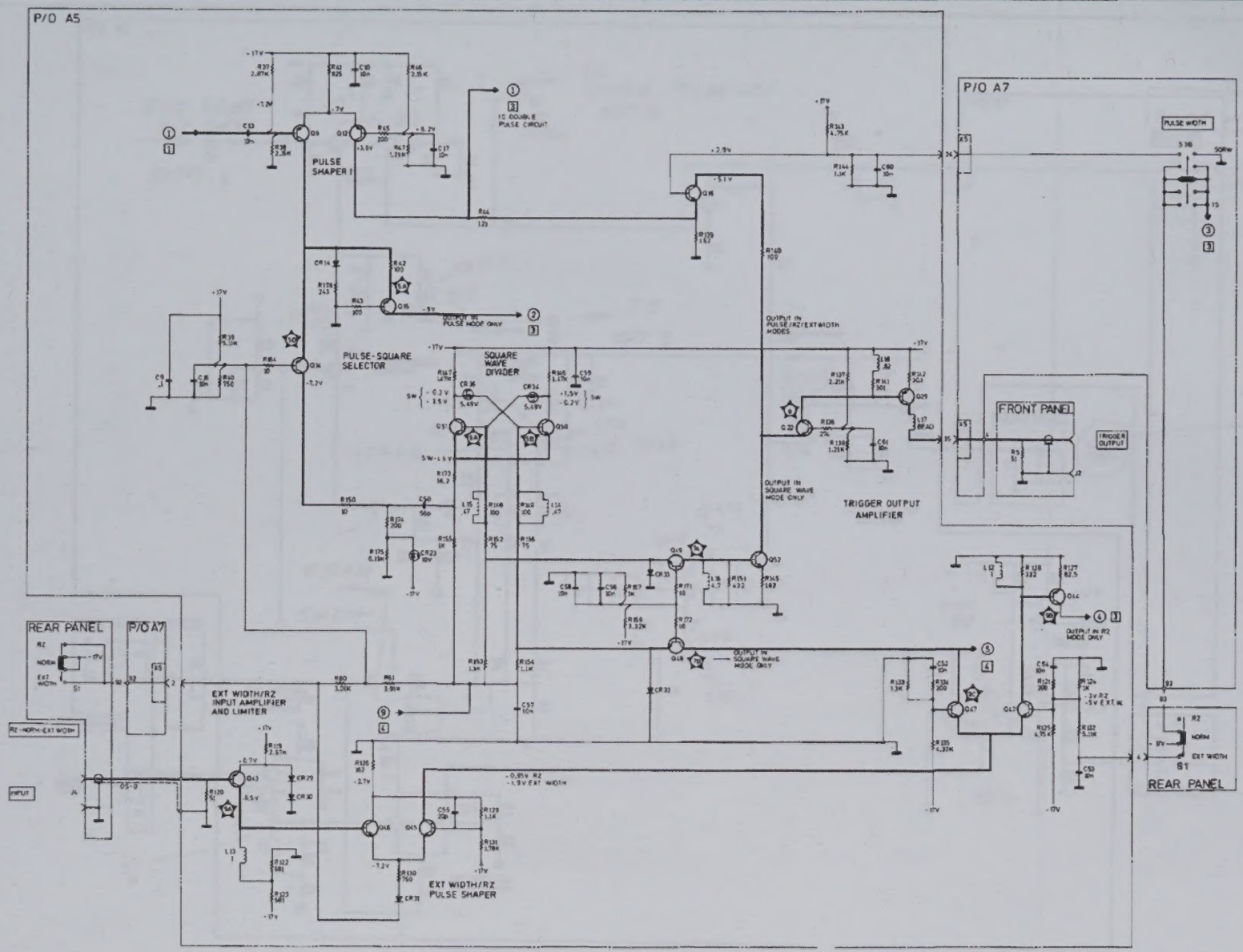
HP 8012B A5 BOARD
PULSE GEN



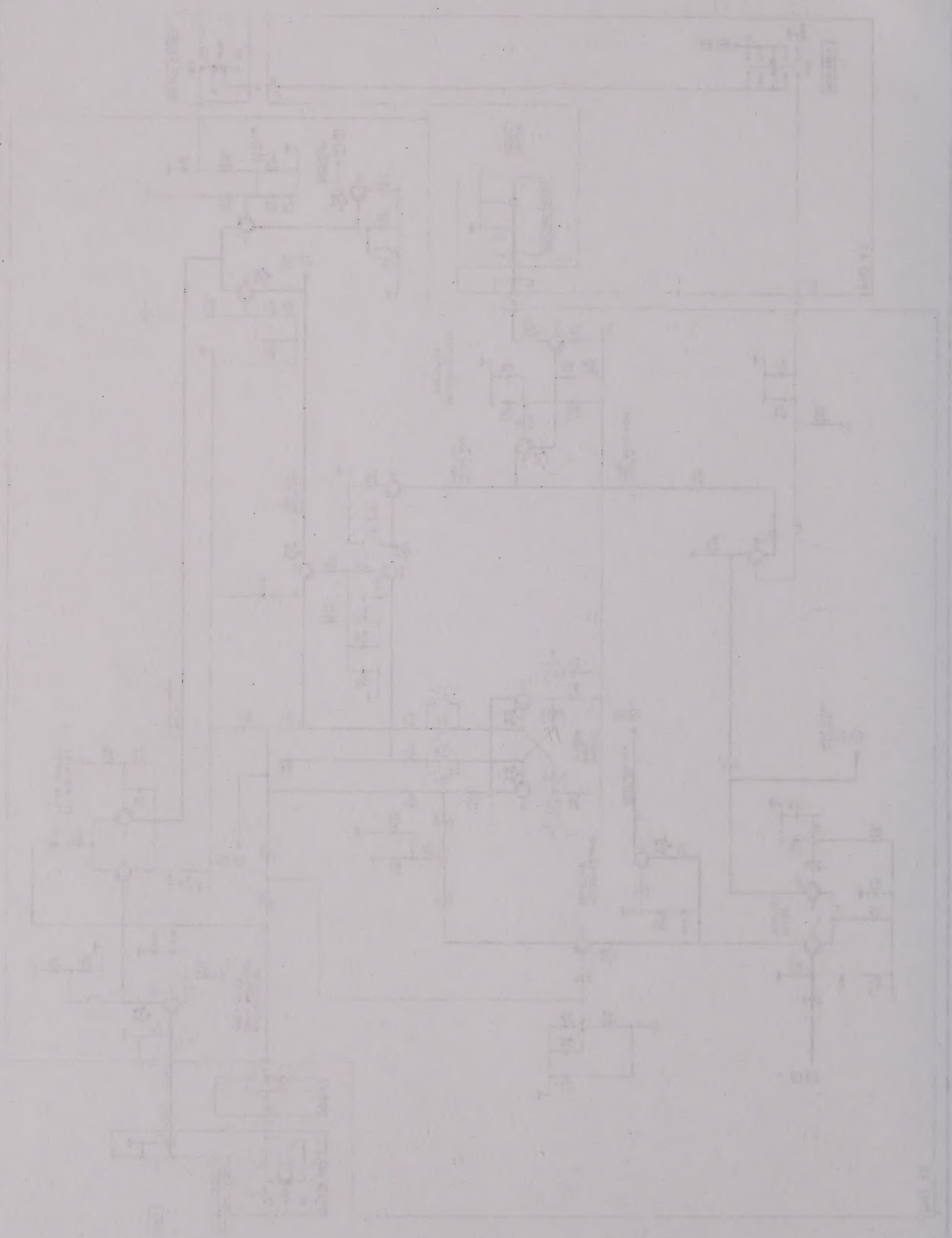
REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	I-3	C22	F-2	C44	B-4	C66	B-2	CR19	C-3	L1	H-3	Q4	H-3	Q26	C-3	Q48	G-5	R15	I-2	R37	E-1	R59	G-3	R82	C-3	R104	B-2	R127	D-3	R149	G-4	R172	G-5
C2	H-3	C23	F-2	C45	B-5			CR20	C-3	L2	H-3	Q5	H-3	Q27	D-2	Q49	H-5	R16	I-2	R38	F-1	R60	E-3	R83	D-3	R105	C-5	R128	D-3	R150	G-4	R173	G-5
C3	I-2	C24	H-2	C46	B-5	C68	I-2	CR21	C-3	L3	F-3	Q6	I-5	Q28	F-3	Q50	G-5	R17	H-3	R39	E-2	R61	G-4	R84	C-3	R106	C-5	R129	F-5	R151	H-5	R174	G-5
C4	I-2	C25	H-2	C47	D-5	C69	E-5	L4	G-2	Q7	H-4	Q29	J-4	Q51	H-5	R18	H-5	R40	E-2	R62	K-3	R85	D-3	R107	C-5	R130	F-4	R152	H-4	R175	G-5
C5	I-3	C26	D-2	C48	C-5	CR1	J-3	CR23	B-5			Q8	I-4	Q30	C-3	Q52	J-5	R19	I-5	R41	E-1	R63	D-2	R86	D-3	R108	C-5	R131	E-5	R153	H-5	R176	E-1
C6	I-2	C27	C-4	C49	D-4	CR2	J-3	CR24	E-5	L6	B-3	Q9	F-2	Q31	D-3	Q53	E-5	R20	H-5	R42	E-1	R64	D-2	R87	C-4	R109	D-5	R132	E-4	R154	G-5	R177	C-2
C7	J-2	C28	D-4	C50	G-5	CR3	J-3	CR25	C-5	L7	C-3	Q10	H-3	Q32	C-4	Q54	E-4	R21	H-5	R43	E-1	R65	C-4	R88	C-4	R110	D-5	R133	E-5	R155	G-5	R178	C-2
C8	F-3	C29	D-1	C51	D-4	CR4	I-3	CR26	C-5	L8	C-4	Q11	G-3	Q33	C-4	Q55	E-4	R22	H-5	R44	E-3	R66	B-2	R89	K-3	R111	C-5	R134	E-5	R156	G-4	R179	C-2
C9	E-3	C30	C-1	C52	E-5	CR5	I-3	CR27	C-5	L9	C-5	Q12	F-3	Q34	D-4	R1	J-3	R23	H-5	R45	E-3	R67	B-3	R90	D-4	R112	D-5	R135	F-5	R157	F-5	R180	C-4
C10	F-3	C31	C-1	C53	E-3	CR6	I-3	CR28	D-5					Q35	B-4	R2	J-2	R24	I-4	R46	E-2	R68	B-2	R91	B-3	R113	D-5	R136	I-5	R158	G-4	R181	B-4
C11	G-3	C32	C-2	C54	F-4	CR7	J-3	CR29	F-4	L11	D-5	Q13	G-3	Q36	B-4	R3	J-2	R25	I-5	R47	E-2	R69	B-2	R92	B-3	R114	E-4	R137	I-5	R159	H-3	R182	B-5
C12	F-3	C33	C-2	C55	F-5	CR8	H-2	CR30	F-4	L12	D-3	Q14	E-2	Q37	B-4	R4	J-2	R26	H-2	R48	H-2	R70	E-2	R93	B-2	R115	E-4	R138	I-5	R160	I-3	R183	F-3
C13	F-2	C34	C-2	C56	G-5	CR9	H-2	CR31	F-4	L13	F-4	Q15	E-2	Q38	D-5	R5	I-2	R27	G-3	R49	F-2	R71	E-1	R94	D-4	R116	E-5	R139	F-3	R161	H-2	R184	G-2
C14	F-3	C35	C-2	C57	H-5	CR10	G-3	CR32	G-4	L14	B-4	Q16	F-3	Q39	D-5	R6	I-2	R28	G-3	R50	G-2	R72	D-1	R95	D-5	R117	D-5	R140	I-4	R162	E-2	R185	G-2
C15	G-3	C36	C-3	C58	H-5	CR11	G-3	CR33	H-5	L15	H-5	Q17	G-2	Q40	C-5	R7	J-3	R29	G-3	R51	I-2	R73	E-1	R96	D-5	R118	F-2	R141	J-5	R163	D-2	R186	H-2
C16	E-2	C37	D-3	C59	G-4	CR12	G-3	CR34	G-4	L16	I-5	Q18	F-2	Q41	D-5	R8	I-3	R30	G-3	R52	F-2	R74	D-1	R97	B-5	R119	F-4	R142	I-5	R164	E-2	R187	E-4
C17	E-2	C38	D-3	C60	E-3	CR13	G-3	CR35	G-4	L17	J-4	Q19	G-2	Q42	E-5	R9	H-3	R31	F-3	R53	G-2	R75	E-1	R98	B-5	R120	F-5	R143	E-3	R165	D-3	R188	E-4
C18	G-2	C39	B-3	C61	I-5	CR14	E-1	CR36	I-4	L18	I-5	Q20	H-2	Q43	F-5	R10	I-3	R32	F-3	R54	F-2	R76	D-1	R99	B-3	R121	F-4	R144	E-3	R166	C-4	R189	E-4
C19	F-1	C40	B-4	C62	H-4	CR15	F-2	CR37	I-5	L19	G-4	Q21	H-2	Q44	D-3	R11	I-3	R33	G-3	R55	G-2	R77	D-2	R100	B-3	R122	F-5	R145	J-5	R167	E-4	R190	F-4
C20	G-2	C41	B-3	C63	I-5	CR16	I-2	CR38	H-5	Q1	J-3	Q22	I-4	Q45	F-5	R12	H-3	R34	F-3	R56	H-2	R78	C-2	R101	B-2	R123	F-5	R146	G-4	R168	E-5	R191	E-4
C21	G-2	C42	B-4	C64	H-3	CR17	G-3	CR39	D-5	Q2	I-3	Q23	D-2	Q46	F-5	R13	I-3			R57	H-2	R79	C-3	R102	B-3	R124	E-5	R147	G-4	R169	E-4	R192	D-3
		C43	B-4	C65	B-5	CR18	B-2	CR40	D-4	Q3	I-3	Q24	D-1	Q47	E-5	R14	I-2	R36	G-3	R58	H-2	R80	C-2	R103	B-3	R125	E-5	R148	H-4	R170	H-5	R193	E-4
								CR41	D-4			Q25	D-2									R81	C-3			R126	F-5			R171	H-5	R199	C-4

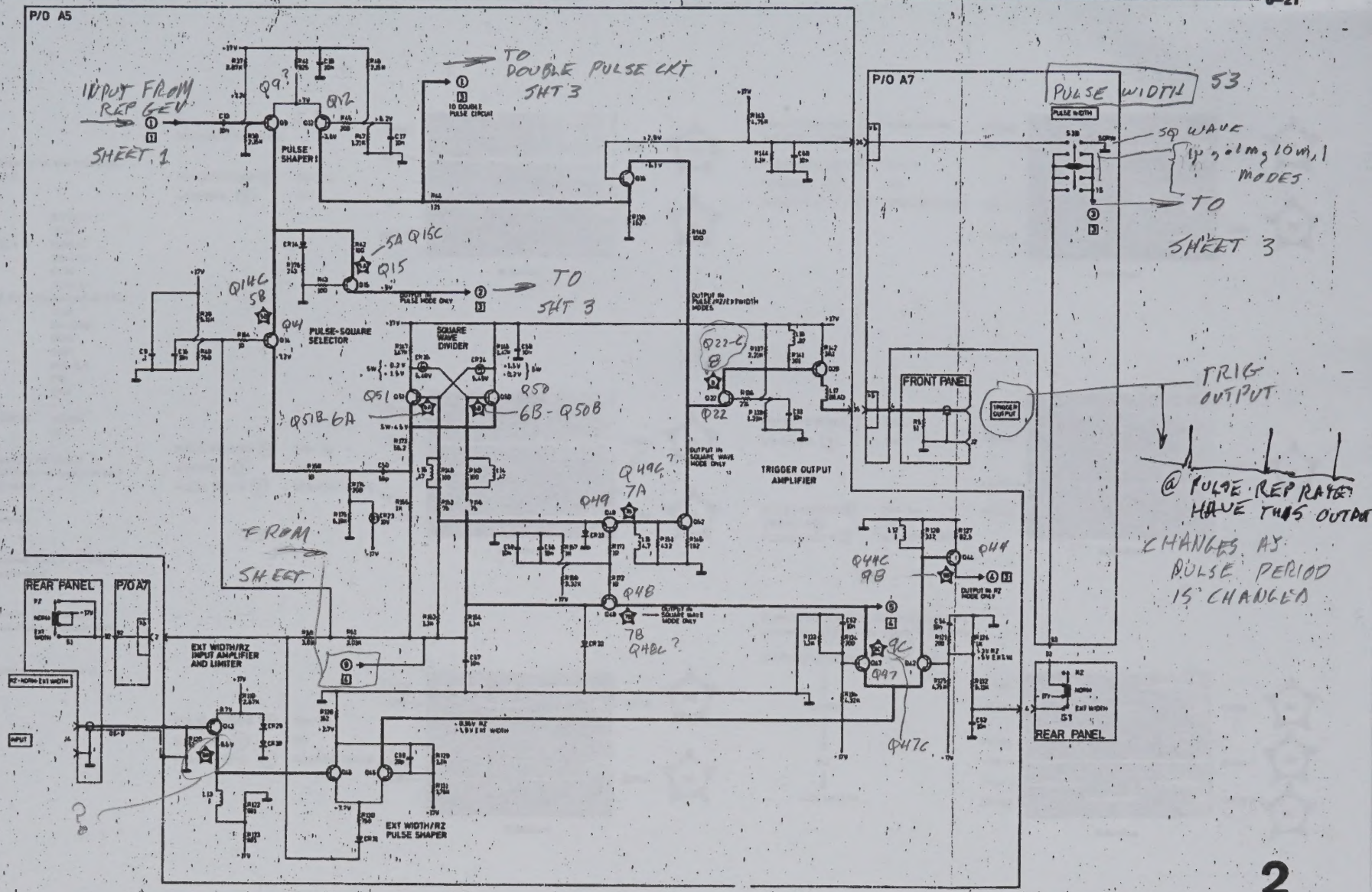
Figure 6-2. Component Layout – Board A5

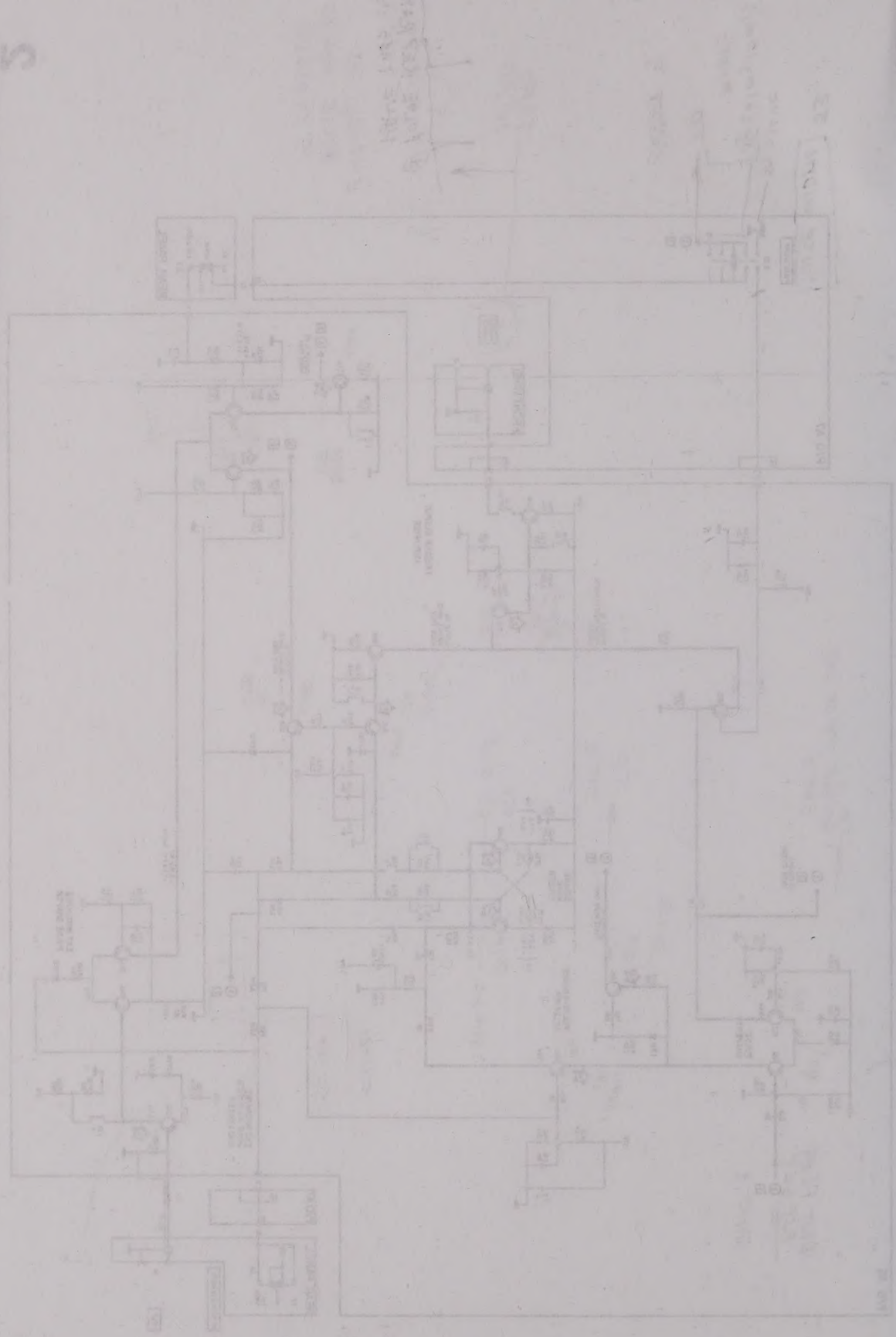


2

MODE SELECTOR, TRIGGER AMPLIFIER, EXT. INPUT AND SQUARE WAVE CIRCUITS 8012B




P/O A5
P/O A7
INPUT FROM REP GEN
SHEET 1
TO DOUBLE PULSE CKT SHT 3
PULSE SHAPER
PULSE-SQUARE SELECTOR
SQUARE WAVE DIVIDER
TRIGGER OUTPUT AMPLIFIER
FRONT PANEL
TRIG OUTPUT
PULSE WIDTH
SQ WAVE
TO SHEET 3
FROM SHEET
REAR PANEL
EXT WIDTH/RZ INPUT AMPLIFIER AND LIMITER
EXT WIDTH/RZ PULSE SHAPER
@ PULSE REP RATES HAVE THIS OUTPUT
CHANGES AS PULSE PERIOD IS CHANGED



NOTES

1. All d.c. voltages were measured with the following pulse settings unless otherwise stated.

PULSE PERIOD 2	EXT(+)
VERNIER 3	CCW
PULSE DOUBLE/NORMAL 4	NORM
PULSE DELAY 5	35n–1μ
VERNIER 6	CCW
PULSE WIDTH 7	10n–1μ
(but set to SQUARE WAVE for voltages marked SW).	
VERNIER 8	CCW
TRANSITION TIME 9	5n–0.5μ
LEADING EDGE 10	CCW
TRAINING EDGE 11	CCW
AMPLITUDE 12	5.0–2.0
VERNIER 13	CW
OFFSET SWITCH 14	OFF
OFFSET VERNIER 15	–
SYM/NORM/COMPL SWITCH 17	NORM
INT LOAD 18	IN
POLARITY 19	+
EXT WIDTH/NORM/RZ SWITCH 24	NORM
(but set to RZ and EXT WIDTH for voltages marked RZ and EXT WIDTH respectively).	

No external input signal required

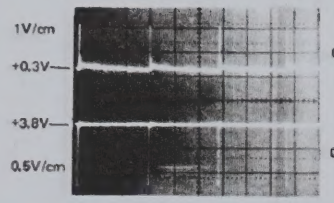
2. A model 3440A digital voltmeter with a 3444A plug-in was used for the d.c. measurements.

3. A model 180C oscilloscope with 1801A and 1821A plug-ins was used for the waveform measurements.

4. A model 8015A pulse generator was used to provide the external input signals.

Pulse settings as for d. c. measurements (see note 1) except for:

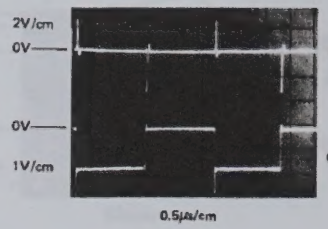
PULSE PERIOD (2) 20n–1μ
VERNIER (3) CW



Q9c 4A
Q12c 4B

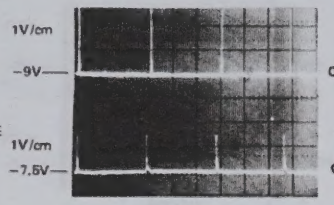
Pulse settings as for d. c. measurements (see note 1) except for:

PULSE PERIOD (2) 20n–1
VERNIER (3) CW
PULSE WIDTH (7) SQUARE WAVE



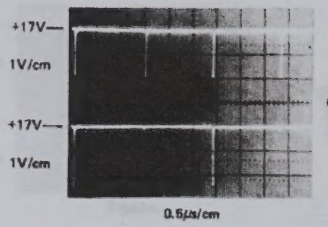
Q49c 7A
Q48c 7B

PULSE PERIOD (2) 20n–1μ
VERNIER (3) CW
PULSE WIDTH (7) SQUARE WAVE



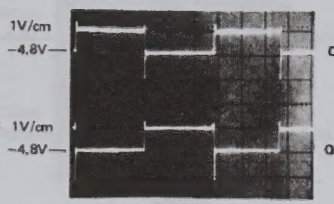
Q15c 5A
Q14c 5B

PULSE PERIOD (2) 20n–1μ
VERNIER (3) CW
PULSE WIDTH (7) SQUARE WAVE



Q22c 8

PULSE PERIOD (2) 20n–1μ
VERNIER (3) CW
PULSE WIDTH (7) SQUARE WAVE

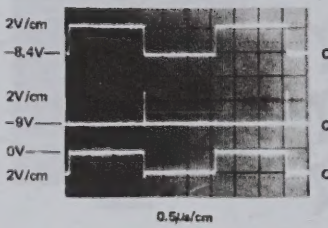


Q51b 6A
Q50b 6B

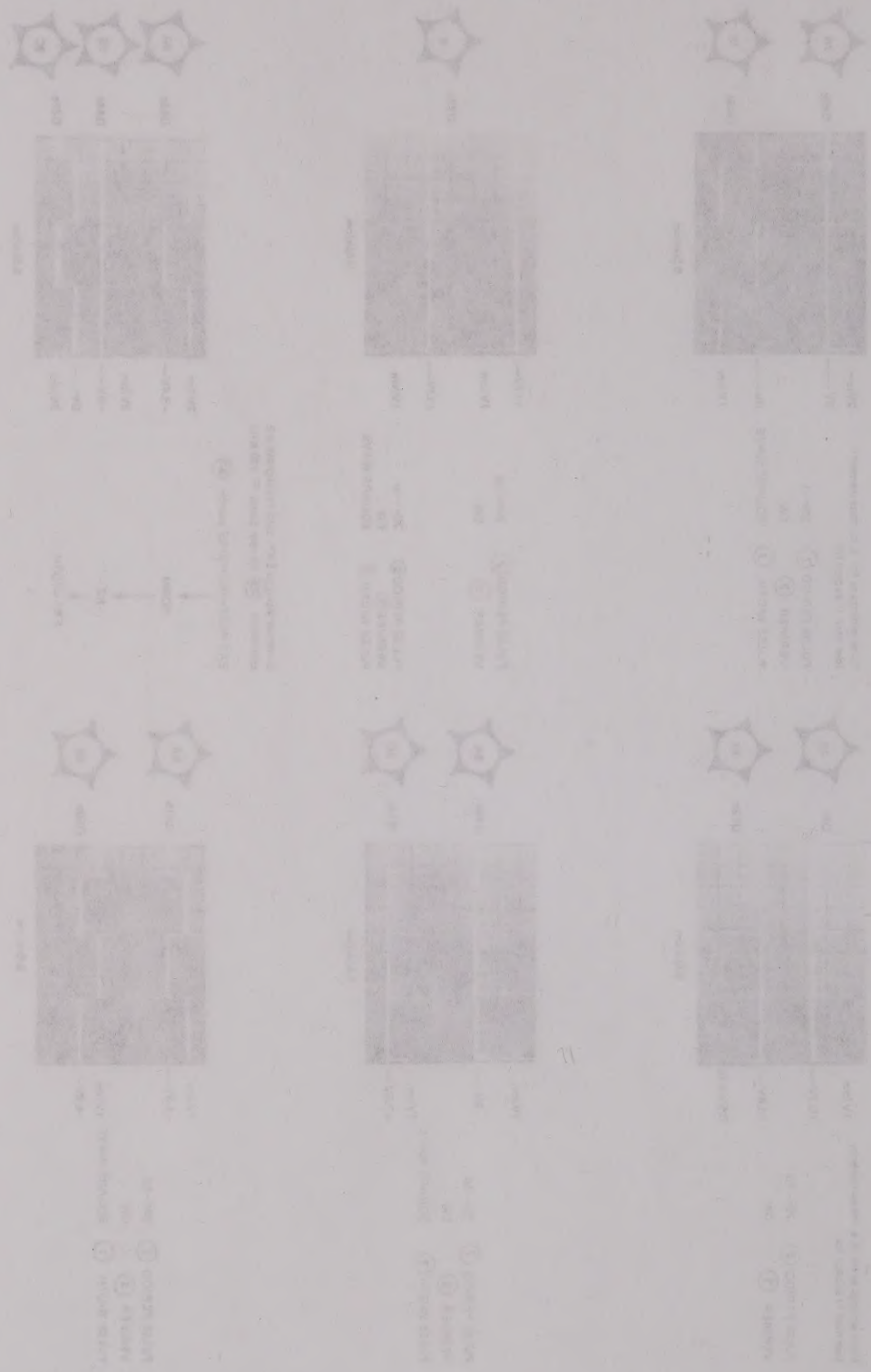
External input to EXT. WIDTH/NORM/RZ connector (25) on rear panel ≙ 330 KHz

EXT WIDTH/NORM/RZ switch (24)

NORM
RZ
EXT WIDTH



Q43c 9A
Q44c 9B
Q47c 9C



MODE SELECT A5 PCB

NOTES

1. All d.c. voltages were measured with the following pulse settings unless otherwise stated.

PULSE PERIOD 2	EXT(+)
VERNIER 3	CCW
PULSE/DOUBLE/NORMAL 4	NORM
PULSE DELAY 5	35n–1μ
VERNIER 6	CCW
PULSE WIDTH 7	10n–1μ
(but set to SQUARE WAVE for voltages marked SW).	
VERNIER 8	CCW
TRANSITION TIME 9	5n–0.5μ
LEADING EDGE 10	CCW
TRAILING EDGE 11	CCW
AMPLITUDE 12	5.0–2.0
VERNIER 13	CW
OFFSET SWITCH 14	OFF
OFFSET VERNIER 15	–
SYM/NORM/COMPL SWITCH 17	NORM
INT LOAD 18	IN
POLARITY 19	+
EXT WIDTH/NORM/RZ SWITCH 24	NORM
(but set to RZ and EXT WIDTH for voltages marked RZ and EXT WIDTH respectively).	

No external input signal required

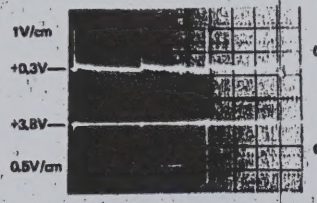
2. A model 3440A digital voltmeter with a 3444A plug-in was used for the d.c. measurements.

3. A model 180C oscilloscope with 1801A and 1821A plug-ins was used for the waveform measurements.

4. A model 8015A pulse generator was used to provide the external input signal.

Pulse settings as for d. c. measurements (see note 1) except for:

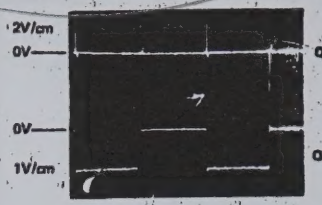
PULSE PERIOD (2) 20n–1μ
VERNIER (3) CW



Q9c (4A) 4A
Q12c (4B) 4B

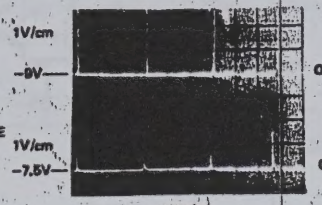
Pulse settings as for d. c. measurements (see note 1) except for:

PULSE PERIOD (2) 20n–1
VERNIER (3) CW
PULSE WIDTH (7) SQUARE WAVE



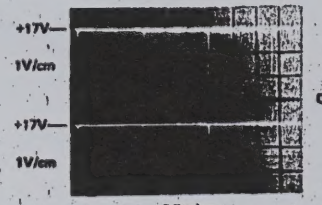
Q49c (7A) 7A
Q48c (7B) 7B

PULSE PERIOD (2) 20n–1μ
VERNIER (3) CW
PULSE WIDTH (7) SQUARE WAVE



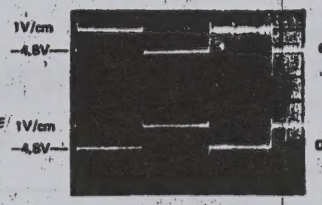
Q15c (5A) 5A
Q14c (5B) 5B

PULSE PERIOD (2) 20n–1μ
VERNIER (3) CW
PULSE WIDTH (7) SQUARE WAVE



Q12c (8) 8

PULSE PERIOD (2) 20n–1μ
VERNIER (3) CW
PULSE WIDTH (7) SQUARE WAVE

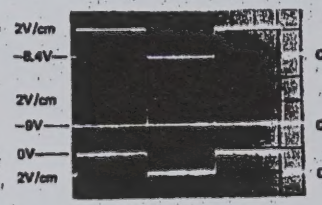


Q51b (6A) 6A
Q50b (6B) 6B

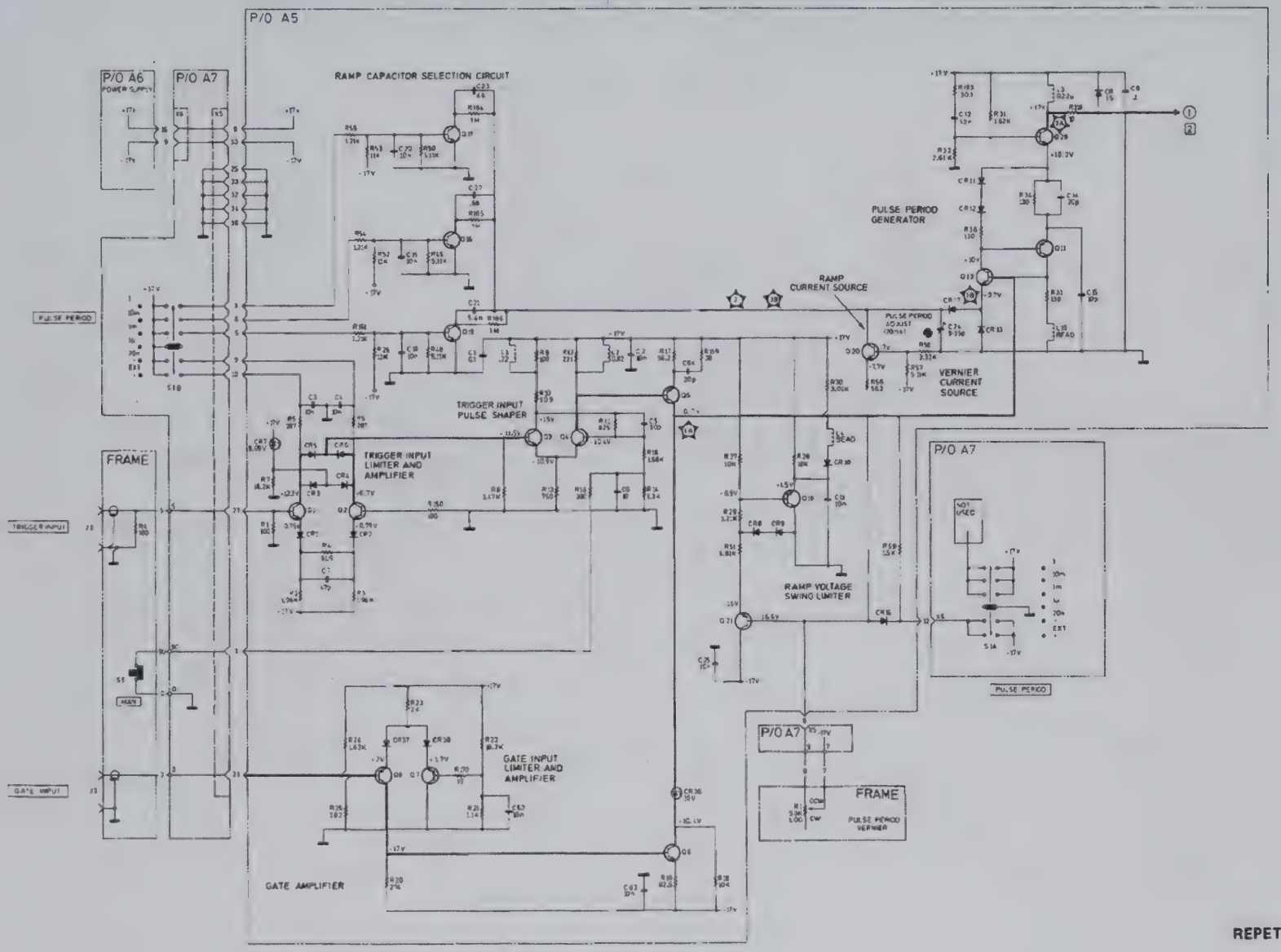
External input to EXT. WIDTH/NORM/RZ connector (25) on rear panel ≙ 330 KHz

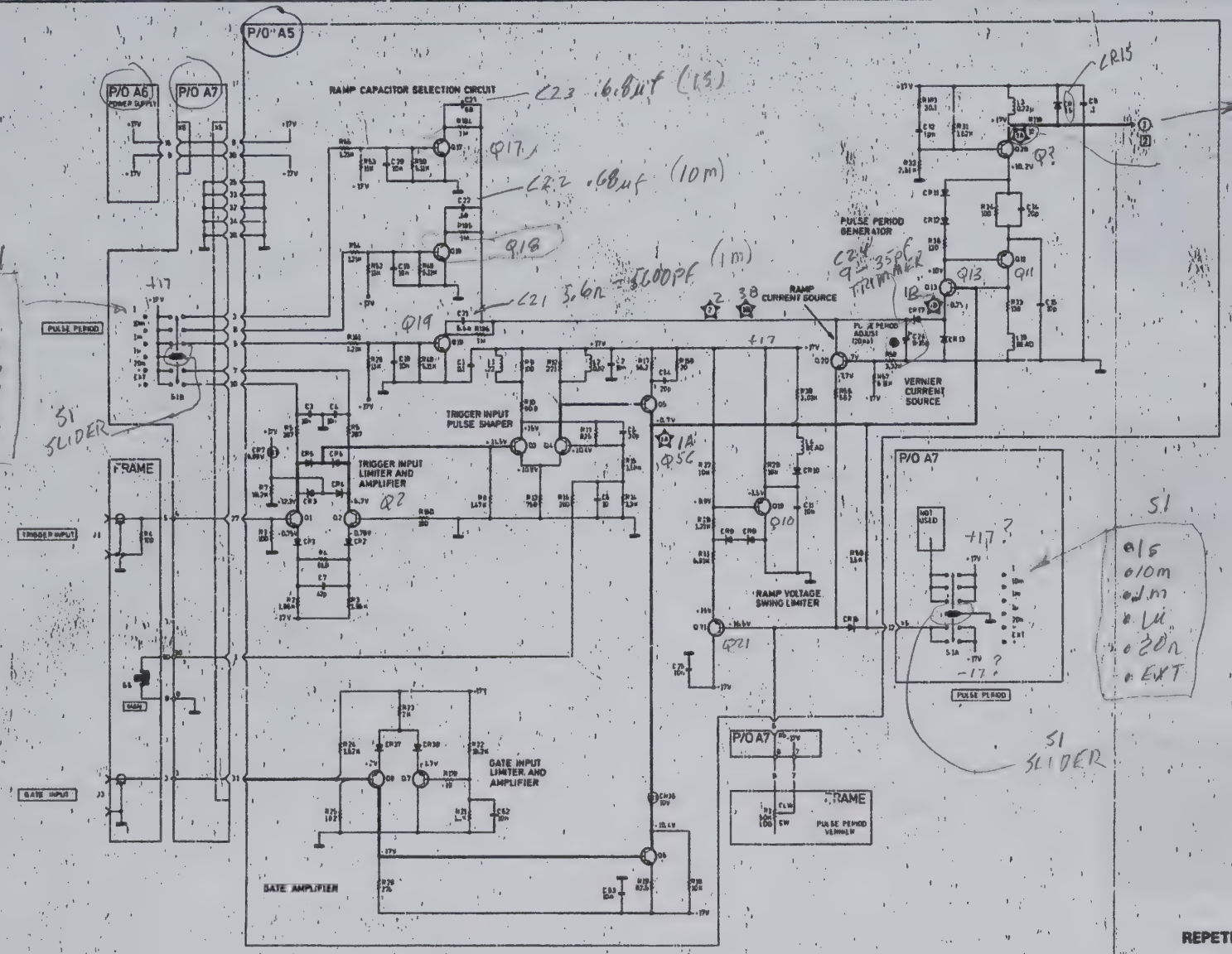
EXT WIDTH/NORM/RZ switch (24)

NORM
RZ
EXT WIDTH



Q43c (9A) 9A
Q44c (9B) 9B
Q47c (9C) 9C


P/O A5
P/O A6
POWER SUPPLY
P/O A7
RAMP CAPACITOR SELECTION CIRCUIT
PULSE PERIOD GENERATOR
RAMP CURRENT SOURCE
PULSE PERIOD ADJUST (20 ns)
VERNIER CURRENT SOURCE
TRIGGER INPUT PULSE SHAPER
TRIGGER INPUT LIMITER AND AMPLIFIER
FRAME
PULSE PERIOD
TRIGGER INPUT
GATE INPUT
MAN
RAMP VOLTAGE SWING LIMITER
GATE INPUT LIMITER AND AMPLIFIER
GATE AMPLIFIER
P/O A7
FRAME
PULSE PERIOD VERNIER
P/O A7
PULSE PERIOD



S1
1s
10m
1m
1µ
20n
EXT

S1 SLIDER

PROBLEMS

1) 1 SEC REP RATE MODE NOT WORKS

OK
SLOPE
1) PULSE PERIODS 20n, 1µ, 1m, 10m WORK

FOR SCHEMATIC G-19 REPRATE GEN

NOTES

1. All d.c. voltages were measured with the following pulse settings unless otherwise stated.

PULSE PERIOD 2	EXT+
VERNIER 3	CCW
PULSE DOUBLE/NORM 4	NORM
PULSE DELAY 5	35n–1μ
VERNIER 6	CCW
PULSE WIDTH 7	10n–1μ
VERNIER 8	CCW
TRANSITION TIME 9	5n–0.5μ
LEADING EDGE 10	CCW
TRAINING EDGE 11	CCW
AMPLITUDE 12	5.0–2.0
VERNIER 13	CW
OFFSET SWITCH 14	OFF
OFFSET VERNIER 15	–
SYM/NORM/COMPL SWITCH 17	NORM
INT LOAD 18	IN
POLARITY 19	+
EXT WIDTH/NORM/RZ SWITCH 24	NORM

No external input signal

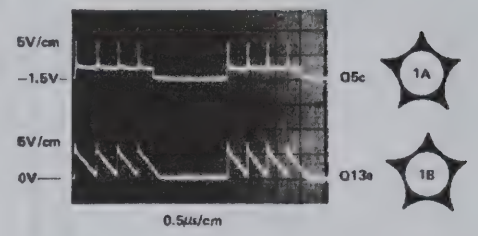
2 A model 3440A digital voltmeter with a 3444A plug-in was used for the d.c. measurements.

3. A model 180C oscilloscope with 1801A and 1821A plug-ins was used for the waveform measurements.

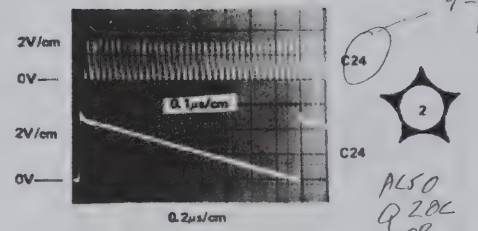
4. A model 8015A pulse generator was used to provide the external input signals.

Pulse settings as for d.c. measurements (see note 1) except for:

EXTERNAL GATE INPUT (21)	330KHz
PULSE PERIOD (2)	20n–1μ
VERNIER (3)	Center



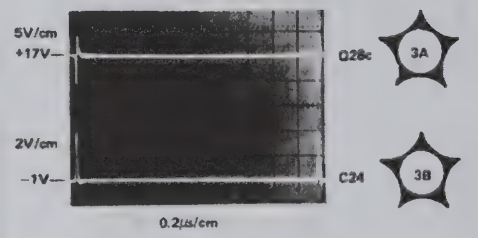
PULSE PERIOD (2)	20n–1μ
VERNIER (3)	CCW
VERNIER (3)	CW



T-33 OR A10 J TRIGGER

ALSO Q20C OR CR17-C

PULSE PERIOD (2) EXT (+)
EXTERNAL TRIGGER INPUT (22)
sine wave ≙ 500 KHz



4–1 INTRODUCTION

4–2 A basic block diagram of the 8012B is shown in Figure 4–1 and this diagram should be referred to when reading the following description. The pulse repetition rate is generated either internally by the rate generator, manually using a push-button, or externally by an applied signal. The pulses thus produced can be gated synchronously by applying an external gating signal to the gate input. The output of the rate generator is fed to the selector circuits and to the trigger amplifier to produce a trigger output.

4–3 The 8012B can be used in one of three modes of operation: Normal mode, RZ mode and External Width mode. In Normal mode the pulses are generated as described above;
In RZ mode external signals, applied directly to the delay generator, determine the repetition rate of the output pulses; In External Width mode external signals, applied to the integrator, determine width and repetition rate of the output pulses. The mode switching is accomplished by the selector circuits.

4–4 The output of the selector circuits, in Normal and RZ modes is applied to the delay generator which delays the pulses by the amount set on the delay controls.

4–5 In dou .e pulse mode two pulses are produced for each trigger pulse; the normal delayed pulse plus an extra pulse that by-passes the delay generator and is thus not delayed.

4–6 The pulse spikes from the delay generator are applied to the width generator where pulses of defined width are created.

4–7 The output of the width generator or, in External Width mode, the external input signal is applied to the integrator where the transition times of the leading and trailing edges are made variable.

4–8 Finally the output of the integrator is amplified, passed through a variable attenuator and has the variable DC offset added.

1Hz → 50MHz REP RATE IN 4 RANGES
SQUARE WAVE .5Hz → 25MHz

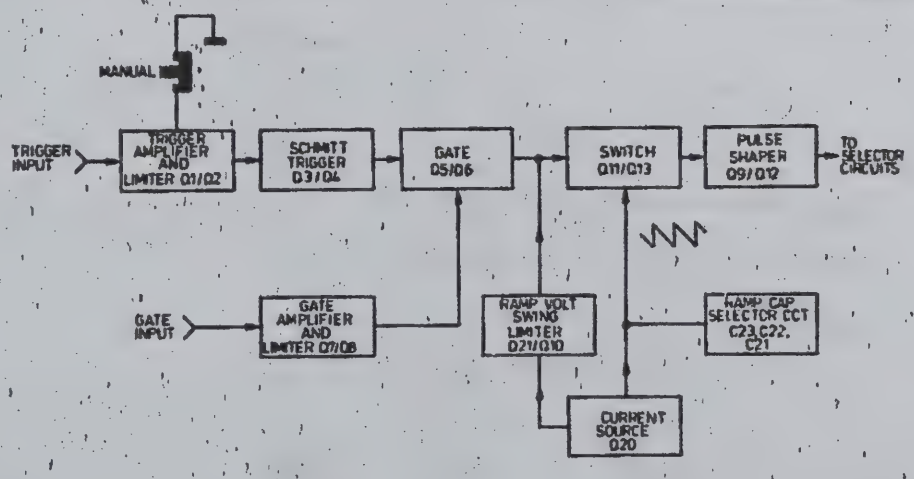


Figure 4–2. Repetition Rate Generator – Block Diagram

4–9 REPETITION RATE GENERATOR

4–10 A block diagram of the repetition rate generator is given in figure 4–2 and a full schematic in diagram 1. These diagrams should be referred to when reading the following description.

4–11 The pulse repetition rate is determined:
a) by the internal rate generator
b) externally using an applied signal
c) manually using a push button.

4–12 Internal rate generator

4–13 When the internal rate generator is used, one of four period ranges is selected using the period range switch. In the three slower ranges, ramp capacitors (C23, C22, C21) are selected to provide the required repetition rate, transistors Q17, Q18 and Q19 switch these capacitors in or out. In the fastest range, no ramp capacitor is switched in; the time is determined by preset capacitor C24. In operation the selected capacitor discharges through constant current sink Q20 controlled by the pulse period vernier R1 and the value of the capacitor. As the voltage at Q20 collector approaches zero, CR17 becomes forward biassed causing Q11 and Q13 to conduct and rapidly recharge the capacitor. The pulse period vernier controls Q21 and Q10 which act as a voltage swing limiter and determine the upper voltage limit to which the ramp capacitor can recharge. When the capacitor has recharged to this limit, Q13 and Q11 cut off thus allowing the discharge cycle to resume. The output from Q11 is applied, via the differentiator network Q28/L3/R35, to the delay generator and the trigger output amplifier.

4–14 External trigger operation

4–15 In external trigger mode the rate gencrator is used as a pulse shaper. Trigger pulses are applied to the differential amplifier Q1/Q2 which in turn switches the Schmitt trigger formed by Q3/Q4. The negative output spikes from the collector of Q4 turn Q5 on and Q13 base rises so that Q13 and Q11 turn on to produce an output pulse.

4–16 Manual operation

4–17 When the manual pushbutton is pressed, a negative spike is produced at the collector of Q4 which enables the current switch Q11/Q13. One pulse is produced from Q11 each time the Manual pushbutton is pressed.

4–18 GATING

4–19 Gate singals are applied to the gate amplifier Q8/Q7. Q8, normally 'off', is turned on by the OV level (off time) of the gate input pulse. Thus Q6 is turned on, the current through Q6 lowers the base voltage of Q13 and so disables the rate generator. When the level of the gate input pulse reaches +1.8V (on time) Q8 turns on and enables the pulse source. Thus output pulses will be produced from the rate generator only during the gate input pulse 'on' time.

4–20 SELECTOR CIRCUITS

4–21 A block diagram of the selector circuits is given in figure 4–3 and is repeated for each mode of operation showing the signal paths used. Figures 4–1, 4–3 and the schematic diagram 2 should be referred to when reading the following description.

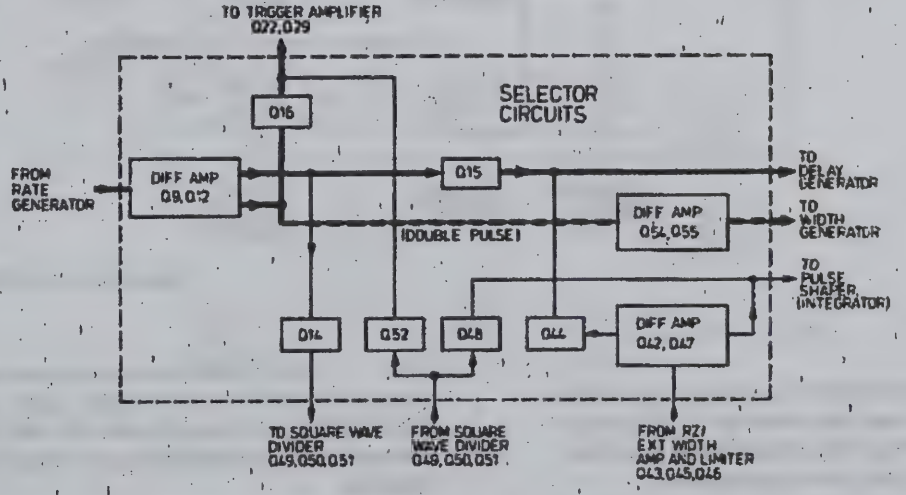


Figure 4–3A Normal Mode (including external trigger and gate mode)

4-22 In Normal mode, the rate generator output is applied to the delay generator via Q15 and to the trigger amplifier via Q16. If double pulse mode is selected, the pulse is also applied to the width generator via differential amplifier Q54/Q55 (see schematic 3).

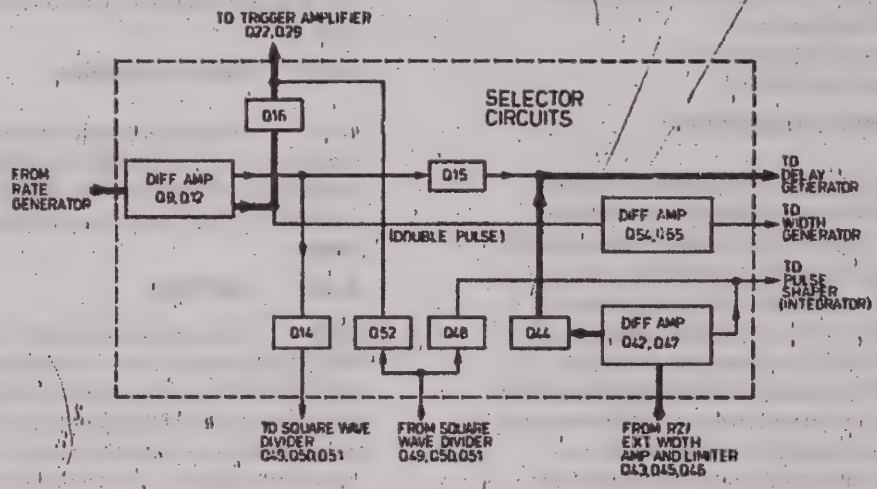


Figure 4--3B RZ Mode

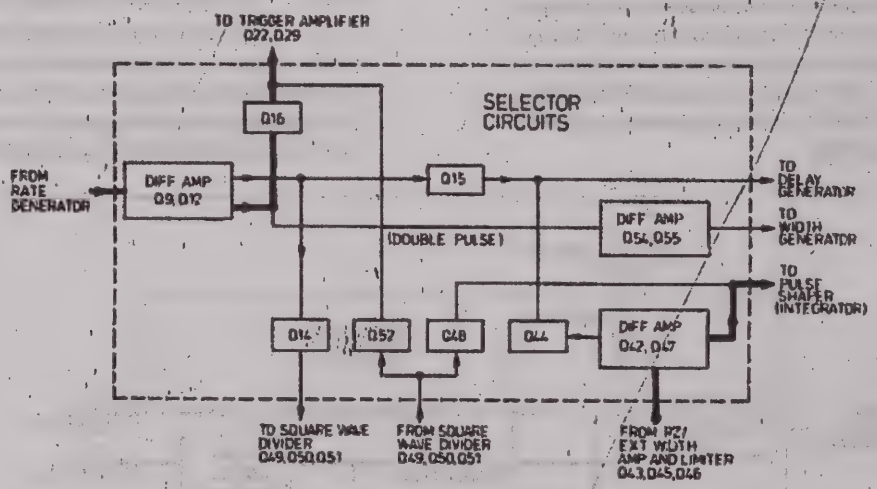


Figure 4-3C. Ext. Width Mode

4-23 In RZ mode the rate generator output is only used to generate trigger pulses, via Q16. The RZ input is applied, via Q43, Q46, Q45 to the differential amplifier Q42/Q47 and gate Q44, to the delay generator.

4-24 In Ext. Width mode the rate generator output is only used to generate trigger pulses, via Q16. The Ext. Width input is applied, via Q43, Q46, Q45 to the differential amplifier Q42/Q47 to pulse shaper 3 and the integrator.

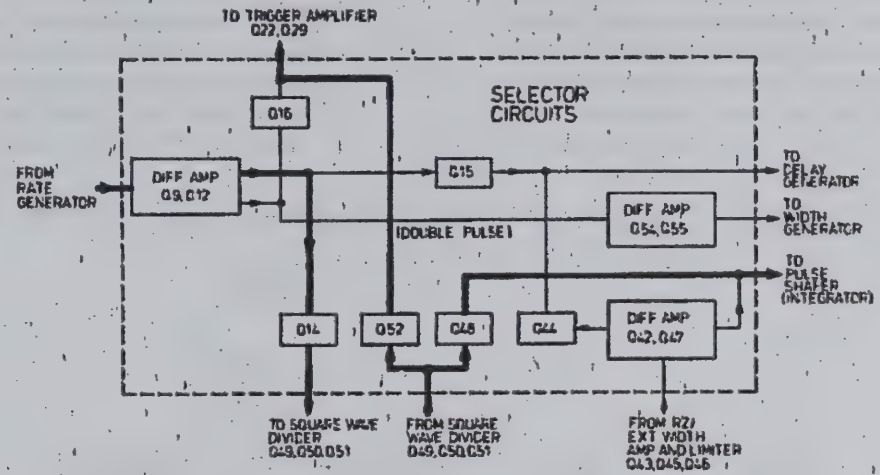


Figure 4–3D Square Wave Mode

4–25 In Square wave mode the output of the rate generator is applied, via Q14, to the square wave divider. The output of the divider is applied to the trigger amplifier, via Q52, and pulse shaper 3 and the integrator, via Q48.

4–26 DELAY GENERATOR

4–27 A block diagram of the delay generator is given in figure 4–4 and a full schematic in diagram 3. These diagrams should be referred to when reading the following description.

4–28 The purpose of the delay generator is to delay the pulse source, whether from the internal rate generator, external trigger or from the RZ input, within the range of 35 ns to 1 s, with respect to the trigger output.

4–29 The current source (Q23), the monostable (Q30/Q31) and the recharge circiut (Q26) are controlled by the width switch so that the delay circuit is inhibited in square wave and external width modes.

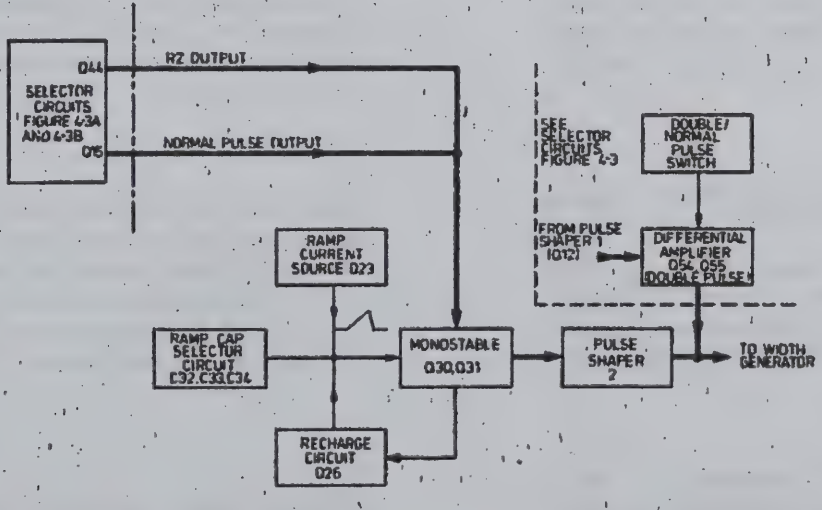


Figure 4–4 Delay Generator – Block Diagram

4–30 Under no-signal conditions, Q31 is off, Q30 is on and Q26 is acting as a sink for the ramp current. Thus the ramp current source (Q23) cannot charge the ramp capacitors. A positive pulse input signal turns Q31 on and Q30 off, Q26 follows Q30 collector and thus is non-conducting. The selected ramp capacitor is charged by the current source Q23 until a level is reached when Q30 turns on again, which turns Q31 off. Q26 now conducts again and rapidly discharges the selected ramp capacitor. The output from the monostable is a negative spike, coincident with the pulse input, followed by a positive spike which occurs some time later and is used to drive pulse shaper 2. The time between the pairs of spikes is the time taken for the ramp waveform to reach the threshold level of the monostable (Q30/Q31), i. e. the delay time.

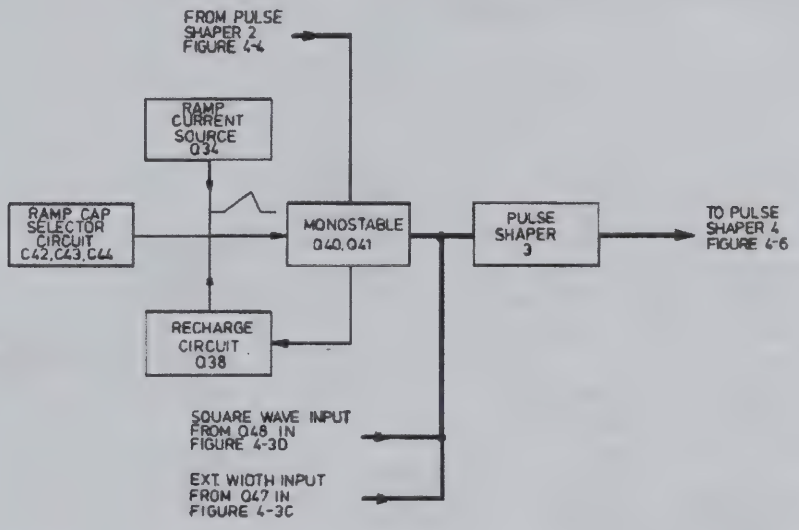


Figure 4–5 Width Generator – Block Diagram

4–31 WIDTH GENERATOR

4–32 A block diagram of the width generator is given in figure 4–5 and a full schematic in diagram 4. These diagrams should be referred to when reading the following description.

4–33 The function of the width generator is to create a pulse of defined width for each positive pulse spike received from the delay generator. The current source (Q34) and the monostable (Q40/Q41) are controlled by the width switch so that the width circuit is inhibited in square wave and external width modes.

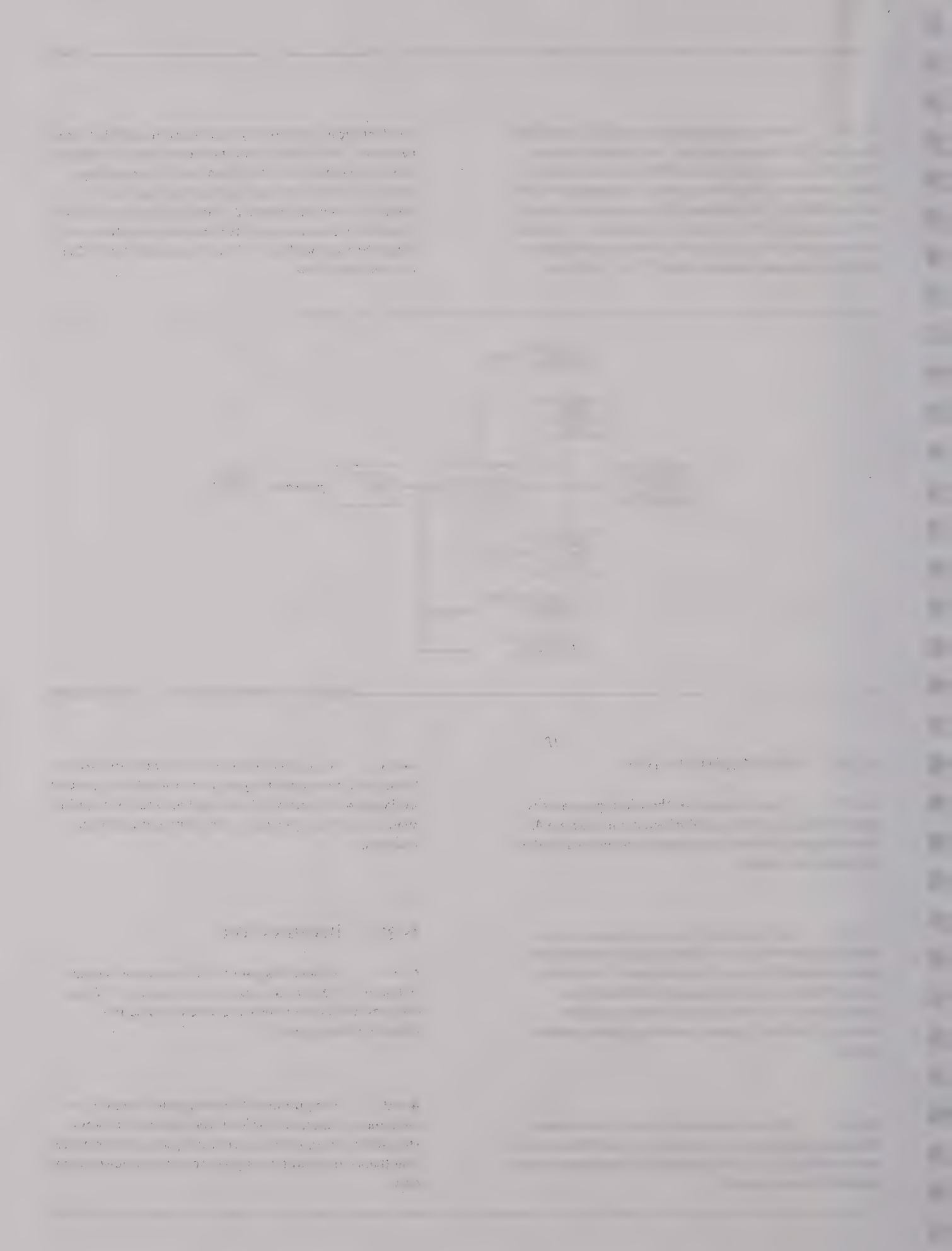
4–34 The width generator circuit is identical to the delay generator circuit except for the differentiator on the output (L11); see para. 4–30. The output pulse is applied to pulse shaper 3.

4–35 If square wave or external width modes are being used, the output signals from the selector circuits in figures 4–3C and 4–3D are applied directly to pulse shaper 3 and both the delay and width generators are disabled.

4–36 INTEGRATOR

4–37 A block diagram of the integrator is given in figure 4–6 and a full schematic in diagram 5. These diagrams should be referred to when reading the following description.

4–38 The purpose of the integrator circuit is, in all modes of operation, to vary the rise and fall times (transition times) of the pulse leading and trailing edges. The theory of operation is given for normal pulse mode only.



4–45 The range capacitor C14 and R41/R42 constitute a low pass filter which is active in the ranges between 0.5 μs and 0.5 s. The filter is turned on and off via CR13/CR14 and CR24 to CR27.

4–46 OUTPUT AMPLIFIER

4–47 A block diagram of the output amplifier is given in figure 4–7 and a full schematic in diagram 6. These diagrams should be referred to when reading the following description.

4–48 The output of the integrator is applied to emitter follower Q13 and then to phase splitter Q15. Transistor Q14 adjusts the symmetry between the leading and trailing edge transition times in the vernier CW position. Roll-off adjustment for positive pulses is achieved using R104/CR17 and for negative pulses using Q17/Q18/R60.

4–49 The appropriate pulse polarity is selected by relay K2 which is controlled via the pulse polarity switch S8.

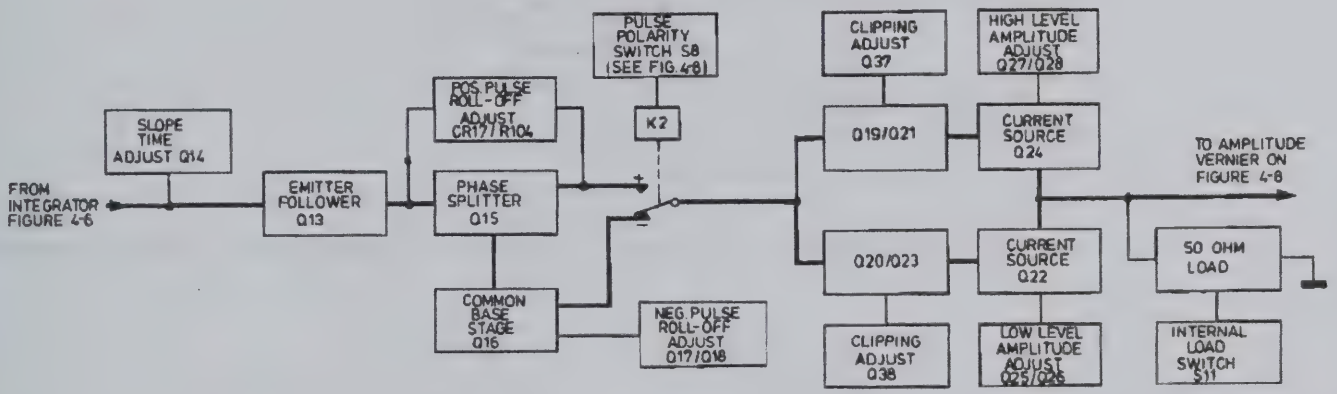


Figure 4–7. Output Amplifier – Block Diagram

4–50 The pulse is then applied to a push-pull amplifier (Q19 to Q24), the output of which is symmetrical about the baseline. High level amplitude adjustment is accomplished by adjusting voltage source Q27/Q28/R88 supplying the common base stage Q24. Low level amplitude adjustment is accomplished by adjusting voltage source Q25/Q26/R87 supplying the common base stage Q22.

4–51 Pulse clipping correction is accomplished by adjusting R69.

4–52 The internal 50 ohm load is switched in or out by the int. load switch via relay K1.

4–53 OFFSETS AND ATTENUATORS

4–54 A block diagram of the offset and attenuator circuits is given in figure 4–8 and a full schematic in diagram 7. These diagrams should be referred to when reading the following description.

4–55 Transistors Q30/Q32 and Q34/Q42 are pulse baseline current sources and the appropriate pair are switched on by the polarity switch. If symmetrical format is selected, both current sources are inhibited.

4–56 Positive and negative pulse baseline adjustment is achieved using R150 and R149 respectively.

4–57 In order to adjust the amplitude and maintain the correct output impedance, a four step attenuator (S7) is used in conjunction with a ganged potentiometer network (R11/R12).

4–58 Transistors Q33, Q39, Q41 and Q48 provide dc offset for the output pulse. If the offset switch (S9) is set to off, transistors Q33 and Q41 are held off and there is no dc offset output. If the offset switch is set to on, the bias on the bases of Q33 and Q41 depends on the

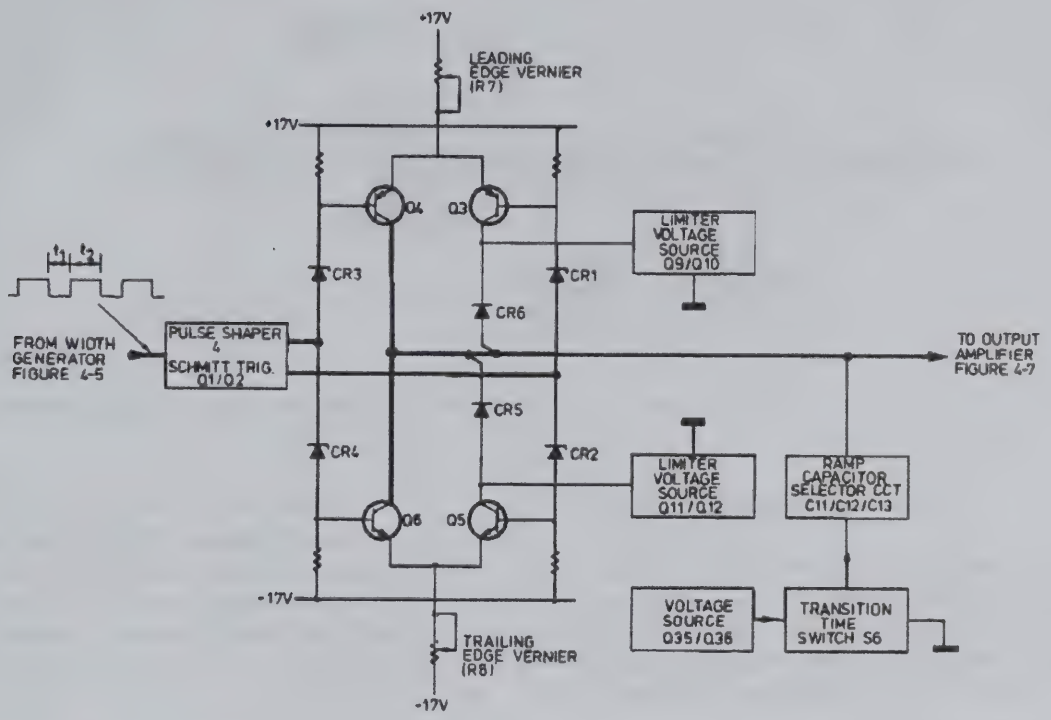
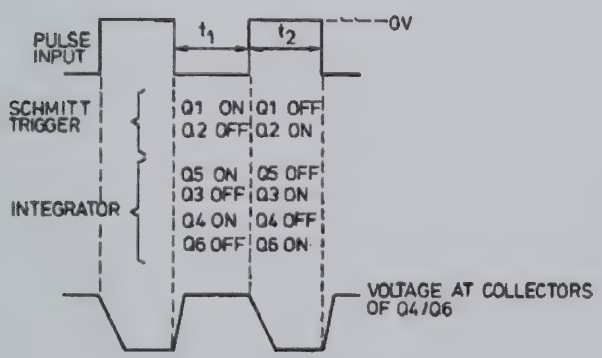


Figure 4–6 Integrator – Block Diagram

4–39 The leading and trailing edges of the pulse from the width generator turn the Schmitt trigger (Q1/Q2) on and off. Transistors Q1 to Q6 turn on and off as follows:



4–40 The leading edge of a pulse (beginning of t_1) switches Q1 on which in turn switches Q4 and Q5 on. Current flows from the +17V line through Q4 and charges the selected ramp capacitor (C11, C12 or C13). The current flow is controlled by the leading edge vernier (R 7). Q5 acts as a current switch and delivers the current from Q11 through Q5 to the –17V line.

4–41 The ramp capacitor charges in a linear manner until CR6 becomes forward biased and begins to conduct via Q9. Thus the pulse top is clamped at a potential defined by the voltage source Q9/Q10.

4–42 At the end of period t_1, Q1 switches off and thus Q4 and Q5 switch off. Q2 switches on which in turn switches Q6 and Q3 on. The selected ramp capacitor now begins to discharge through Q6 to the –17V line. The current flow is controlled by the trailing edge vernier (R 8). Q3 acts as a current switch and supplies current from the +17V line to Q9.

4–43 The ramp capacitor discharges in a linear manner until CR5 becomes forward biassed and begins to conduct via Q11. Thus the pulse base is clamped at a potential defined by the voltage source Q11/Q12. The cycle is repeated when, at the end of t_2, Q2 turns off and Q1 turns on again.

4–44 The voltage source Q35/Q36 supplies the reference voltage for switching the ramp capacitors.

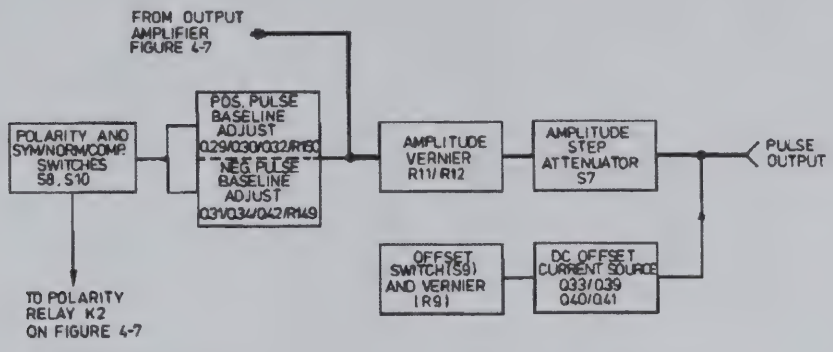


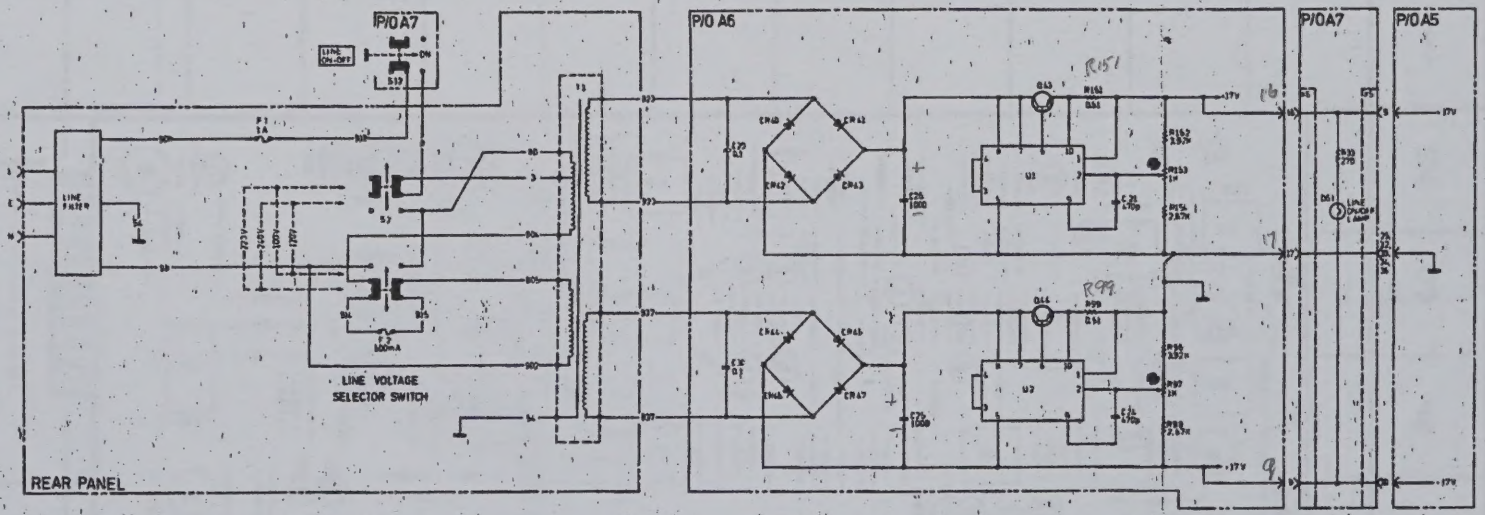
Figure 4–8 Offsets and Attenuators — Block Diagram

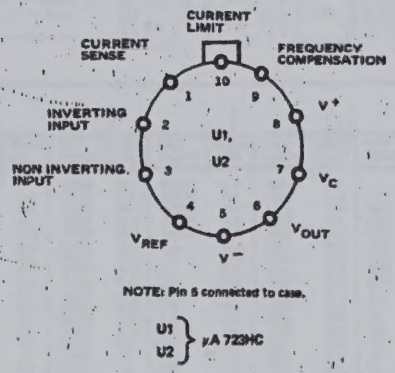
setting of the offset vernier (R9). As the vernier is turned counter clockwise Q33 is turned off and Q41 is turned on supplying a negative offset current. As the vernier is turned clockwise Q41 is turned off and Q33 is turned on supplying a positive offset current. The current is applied to an output load (L1 to L4, R8 to R10).

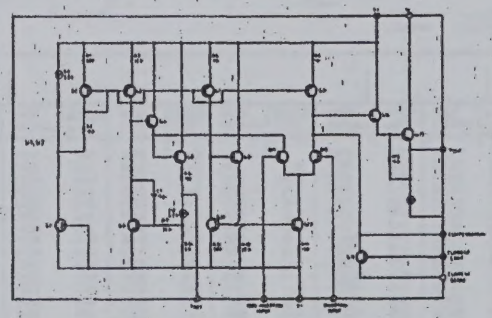
4–59 POWER SUPPLIES

4–60 The +17V and –17V power supplies are identical series regulated types using IC regulators (U1 and U2) and series pass transistors (Q43 and Q44). Resistors R151 and R99 act as current sensing resistors to enable the regulators to limit the current output.

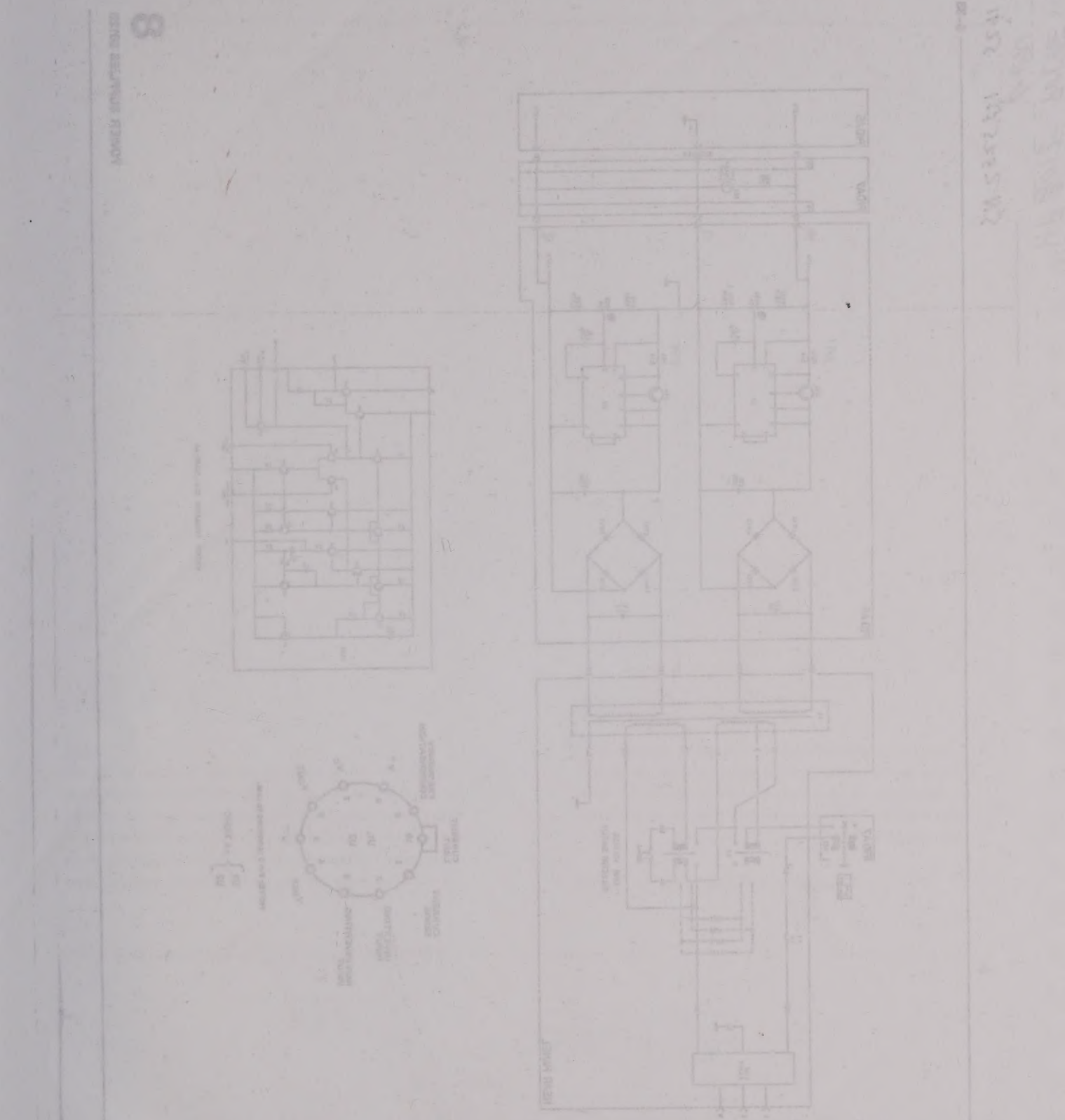
HP 8012 PULSE GEN
SN 2325A1 5291



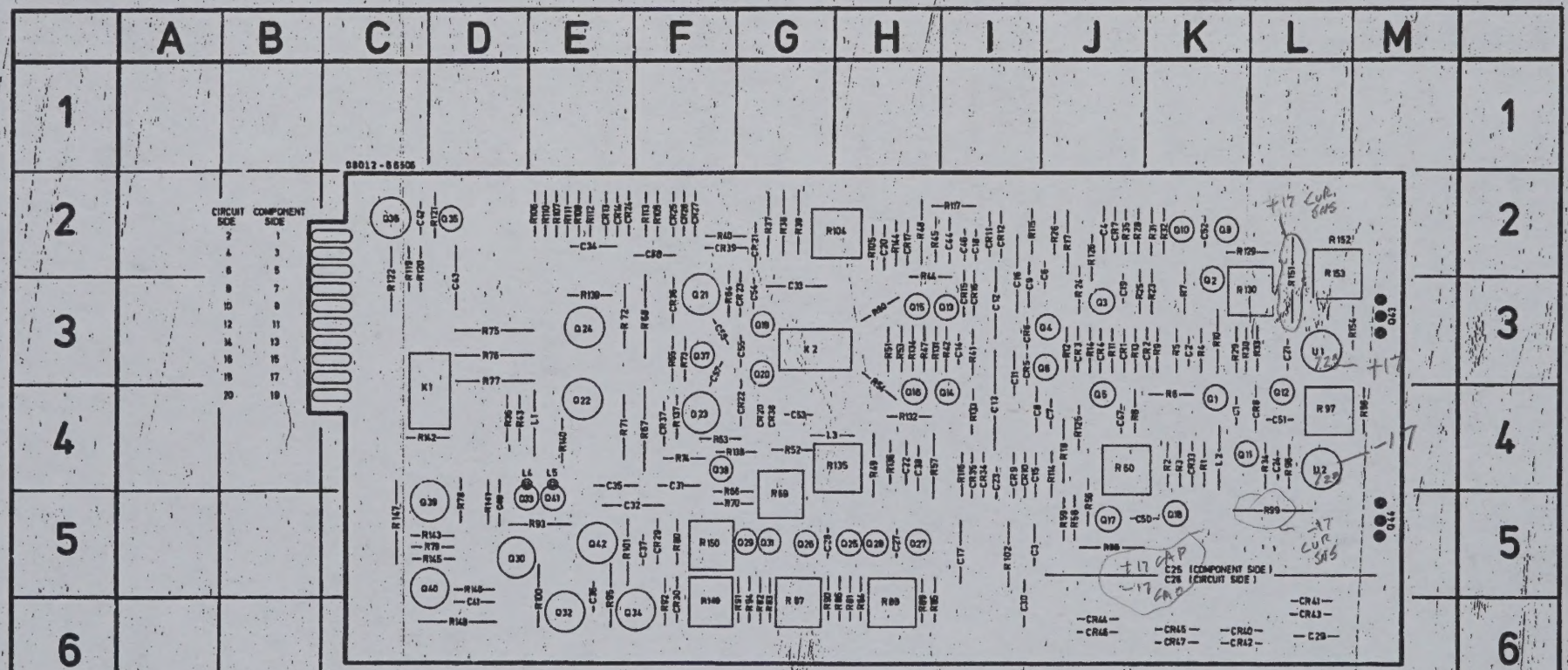




VOLTAGE REGULATOR IC's – BOARD A6



HP 8012 PULSE GEN



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C1	K-4	C26	K-5	C51	L-4	CR15	I-3	CR43	L-6	Q14	I-4	Q37	F-3	R17	J-2	R45	H-2	R71	E-4	R93	E-5	R117	I-2	R145	D-5
C2	K-3	C27	K-5	C52	K-2	CR16	I-3	CR44	J-6	Q15	H-3	Q38	F-4	R18	J-3	R46	H-2	R72	E-3	R94	G-5	R118	I-2	R146	D-5
C3	J-5	C28	K-5	C53	G-4	CR17	H-2	CR45	K-6	Q16	H-4	Q39	D-5	R24	J-3	R47	H-2	R73	F-3	R95	E-6	R119	C-2	R147	C-5
C4	J-2	C29	L-6	C54	G-3	CR20	G-4	CR46	J-6	Q17	J-5	Q40	D-5	R25	J-3	R48	H-3	R74	F-4	R96	E-6	R120	C-2	R148	D-6
C5	J-4	C30	L-6	C55	G-3	CR21	G-2	CR47	K-6	Q18	K-5	Q41	E-5	R26	J-2	R49	H-3	R75	D-3	R97	L-4	R121	D-2	R149	F-6
C6	J-4	C31	K-5	C56	F-3	CR22	G-4	K1	C-4	Q19	G-3	Q42	E-5	R28	J-2	R50	H-3	R76	D-3	R98	M-4	R122	C-3	R150	F-5
C7	J-3	C32	K-4	C57	F-3	CR23	G-3	K2	G-3	Q20	G-3	Q43	M-3	R29	K-3	R51	H-3	R77	D-3	R99	L-5	R125	J-4	R151	L-2
C8	J-3	C33	K-4	C58	F-2	CR24	E-2	L1	L-3	Q21	F-3	Q44	M-5	R30	K-3	R52	G-4	R78	D-5	R100	E-6	R126	J-2	R152	L-2
C9	J-3	C34	E-2	C59	F-2	CR25	F-2	L2	L-3	Q22	E-4	Q43	M-3	R31	K-4	R53	H-3	R79	D-5	R101	E-5	R129	K-2	R153	L-2
C10	J-3	C35	K-3	CR1	L-3	CR26	F-2	L3	L-4	Q23	E-4	Q44	M-5	R32	K-4	R54	H-4	R80	D-5	R102	I-5	R130	K-3	R154	L-3
C11	J-3	C36	K-3	CR2	K-3	CR27	F-2	L4	L-4	Q24	E-4	R1	K-4	R33	K-3	R55	J-5	R81	H-2	R104	H-2	R131	K-3	U1	L-3
C12	J-3	C37	E-5	CR3	J-2	CR29	F-5	L5	L-5	Q25	E-4	R2	K-4	R34	K-3	R56	H-4	R82	H-2	R105	E-2	R132	H-3	U2	L-4
C13	J-3	C38	F-5	CR4	J-3	CR30	F-6	Q1	K-4	Q26	G-5	R3	K-4	R35	J-2	R57	H-4	R83	H-2	R106	E-2	R133	I-4		
C14	J-3	C39	H-4	CR5	I-3	CR33	K-4	Q2	K-3	Q27	H-5	R4	K-3	R36	D-4	R58	J-5	R84	G-5	R107	E-2	R134	H-4		
C15	J-3	C40	D-5	CR6	I-3	CR34	I-4	Q3	K-3	Q28	H-5	R5	K-4	R37	G-2	R59	J-5	R85	H-6	R108	E-2	R135	H-4		
C16	J-3	C41	D-6	CR7	I-2	CR35	I-4	Q4	K-3	Q29	G-5	R6	K-3	R38	G-2	R60	J-4	R86	H-6	R109	F-2	R136	H-4		
C17	J-3	C42	D-5	CR8	L-4	CR36	F-3	Q5	K-4	Q30	D-5	R7	K-3	R39	G-2	R63	F-4	R87	G-5	R110	E-2	R137	F-4		
C18	J-2	C43	D-5	CR9	I-4	CR37	F-4	Q6	K-3	Q31	G-5	R8	K-3	R40	F-2	R64	F-3	R88	H-6	R111	E-2	R138	F-3		
C19	J-2	C44	I-2	CR10	I-4	CR38	G-4	Q7	K-3	Q32	E-6	R9	J-4	R41	G-2	R65	F-3	R89	H-6	R112	E-2	R139	E-4		
C20	J-2			CR11	I-2	CR39	F-2	Q8	K-3	Q33	D-5	R10	K-3	R42	F-2	R66	F-4	R90	H-6	R113	F-2	R140	E-4		
C21	J-2	C45	I-2	CR12	I-2	CR40	K-6	Q9	K-3	Q34	F-6	R11	J-3	R43	I-3	R67	F-3	R91	H-5	R114	J-4	R141	D-5		
C22	J-2	C47	I-4	CR13	E-2	CR41	L-6	Q10	K-2	Q35	D-2	R12	J-3	R44	H-3	R68	G-5	R92	G-5	R115	I-2	R142	C-4		
C23	J-2	C50	I-4	CR14	E-2	CR42	K-6	Q11	K-2	Q36	C-2	R13	J-3			R69	F-5		F-6	R116	I-4	R143	D-5		
C24	J-2							Q12	L-4			R14	J-3			R70						R144	H-2		
C25	K-5							Q13	I-3																

Figure 6–3. Component Layout – Board A6